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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,591	03/19/2004	Daniel L. W. Chieng	D2A1240-1	9251

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EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,591	CHIENG ET AL.	
	Examiner	Art Unit	
	Naheed Ejaz	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 8, 11, 15 & 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) (hereinafter, Rabenko) in view of Oltean (6,044,113).

3. As per claim 1, Rabenko teaches, 'a clock source' (figure 17, element 'Crystal_24.576MHz_clock', col.30, lines 14-17), 'a first counter coupled to receive a clock signal from the clock source and configured to count cycles of the clock signal in a sample period corresponding to a first digital data stream' (figure 17, elements 556, 560 & 557, col.30, lines 20-24), 'a second counter coupled to receive the clock signal from the clock source and configured to count cycles of the clock signal in a sample period' (figure 17, elements 558 & 556, col.30, lines 14-24), 'a data processor (figure 17, element 554) coupled to the first and second counters and configured to read a first number of cycles counted by the first counter and a second number of cycles counted by the second counter' (figure 17, elements 556, 557 & 554, col.30, lines 24-31) (it is noted that Sampling-rate tracker 554 (figure 17) is coupled to counters 556 & 557 and process data by reading counts A & B in order to calculate ratio so that sampling rate is calculated which is equivalent to the claim limitations of having a data processor

coupled to first and second counters and reads first and second number of cycles counted by first and second counter respectively), 'convert at least one of the first and second digital data streams from a corresponding input sample rate to a predetermined sample rate based on the number of cycles counted in the corresponding digital data stream' (figure 17, elements 554, col.30, lines 24-33) (it is noted that Sampling-rate tracker 554 (figure 17) uses input and output sampling counts 1,2,3 & 4 and A, B, C, & D in order to resample the incoming signal at the predetermined/calculated rate (figure 17B, col.30, lines 37-47) which reads on the claim limitations).

Although Rabenko teaches that counter_B (claimed second counter) outputs the count of the clock signal to the sampling rate tracker in order to compare ratio of count_A with count_B (figure 17, col.30, lines 14-31) but he fails to disclose second counter count cycles of the clock signal *corresponding to a second digital data stream.*

Oltean teaches digital pulse modulation scheme 100 (figure 1) that uses two counters 106(a) and 106(b) (figure 1) (claimed first counter and second counter respectively) and both of them have input from clock source 102 and perform a modulo-N counts at each clock pulse in order to count cycles (col.1, lines 27-36 & 39-48) (claimed 'a first counter coupled to receive a clock signal from the clock source and configured to count cycles of the clock signal') and based on these counts, output two N1 and N pulses (col.1, lines 34-38) (claimed 'first digital data stream' & 'second digital data stream') which are digital since in digital pulse width modulation, a digital input is counted and used to generate train of pulses (col.1, lines 21-24).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Oltean into Rabenko in order to produce precise and stable duty cycle for providing control to complex electronic devices as taught by Oltean (col.1, lines 3-5 & 54-57).

4. As per claim 3, Rabenko teaches, 'a low-pass filter configured to filter the first number of cycles and the second number of cycles' (figure 17, elements 563 & 563', col.30, lines 18-24).

5. As per claim 8, Rabenko discloses, 'estimate a primary rate for the first digital data stream based upon the cycles counted by the first counter' (figure 17, elements 556 & 557), 'estimate a secondary rate for the second digital data stream based upon a ratio of the cycles counted by the second counter to the cycles counted by the first counter' (figure 17, element 554, col.30, lines 24-31).

6. Claim 11 is rejected under the same rationale as mentioned in the rejection of claim 1 above.

7. Claim 15 is rejected under the same rationale as mentioned in the rejection of claim 8 above.

8. Claim 18 is rejected under the same rationale as mentioned in the rejection of claim 3 above.

9. Claims 2, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) in view of Oltean (6,044,113), as applied to claims 1 & 11 above, and further in view of Araki (2003/0037297).

10. As per claim 2, Rabenko and Oltean teach all the limitations in the previous claims on which claim 2 depends but they fail to disclose incrementing first and second counters after frame sync is received. Oltean teaches first counter configured to count cycles corresponding to the first digital data stream and second counter configured to count cycles corresponding to the second digital data stream (see claim 1 rejection above).

Araki teaches incrementing first counter once for each cycle after a frame sync signal is received in the first digital data stream (see figures 3 or 5, elements S2, S4, S5) and incrementing of second counter once for each cycle after a frame sync signal is received in the second digital data stream (figures 3 or 5, elements S15, S16).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Araki into Rabenko and Oltean in order to establish frame synchronization as taught by Araki (col.1, paragraph # 0002).

11. Claim 12 is rejected under the same rationale as mentioned in the rejection of claim 2 above.

12. As per claim 13, in addition to aforementioned rejection of claim 12, Rabenko and Araki teach all the limitations in the previous claims on which claim 13 depends but they fail to disclose counting of first value and second value from the first and second counter respectively.

Oltean teaches that counter 106(a) counts N1 which includes first value of the counter as well (claimed reading first value from the first counter) (figure 1,col.1, lines 30-36) and counter 106(b) counts N pulses which includes second value of the counter

as well (claimed reading second number of cycles for the second digital data stream comprises reading a second value from the second counter) (figure 1, col.1, lines 30-36) at each clock pulse.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Oltean into Rabenko in order to produce precise and stable duty cycle for providing control to complex electronic devices as taught by Oltean (col.1, lines 3-5 & 54-57).

13. Claims 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) in view of Oltean (6,044,113), as applied to claims 1, 8, 11 & 15 above, and further in view of Holland et al. (5,367,162) (hereinafter, Holland).

14. As per claim 9, Rabenko and Oltean teach all the limitations in the previous claims on which claim 9 depends but they fail to disclose first and second FIFO to store digital data streams.

Holland teaches, 'first FIFO and a second FIFO (figure 5, elements 86 & 92, col.6, lines 43-49), wherein data from the first digital data stream is stored in the first FIFO (figure 5, elements 84 & 86, col.15, lines 43-46) and data from the second digital data stream is stored in the second FIFO' (figure 5, elements 90 & 92, col. 15, lines 50-52).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Holland into Rabenko and Oltean in order to maximizes system throughput while one FIFO buffer is filled the other one is read out by digital signal processor as taught by Holland (col.16, lines 35-43).

15. Claim 16 is rejected under the same rationale as mentioned in the rejection of claim 9 above.

16. Claims 4 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) in view of Oltean (6,044,113), as applied to claims 1 & 11 above, and further in view of LaMacchia (6,393,198).

17. As per claim 4, Rabenko and Oltean teach all the limitations in the previous claim on which claim 4 depends but they fail to disclose resetting of first and second counters each time sync signal is received.

LaMacchia teaches, 'data processor is configured to reset the first and second counters each time a succeeding frame sync signal is received' (figure 3, elements 42, 114, 116, figure 6, col.12, lines 62-67, col.13, line 1 & 10-22, col.17, lines 35-47) (it is noted that LaMacchia uses RTS command to rest counters (col.17,lines 22-24) which is based on the detection of synchronization of frame by using the GET_SC_THISFRAME command packet (col.17, lines 35-63) and is equivalent to claim limitations).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of LaMacchia into Rabenko and Oltean in order to reset counters at the digital workstation (digital system) because counters are accurately aligned, trigger positions without introducing variable delays in the digital system which is inherent in software triggering as taught by LaMacchia (col.4, lines 1-11).

18. Claim 14 is rejected under the same rationale as mentioned in the rejection of claim 4 above.

19. Claims 5, 6, 7 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) in view of Oltean (6,044,113), as applied to claims 1 & 11 above, and further in view of Loh et al. (5,621,805) (hereinafter, Loh).

20. As per claim 5, Rabenko and Oltean teach all the limitations in the previous claim on which claim 5 depends but they fail to disclose first and second digital data not restricted to a set of predetermined sample rates.

Loh teaches that the sampling rate output depends on input digital data on each channel which are sampled at an arbitrary rate (col.6, lines 27-32) therefore, the input digital data of Loh is not restricted to any sample rate because it's arbitrary and thus reads on claim limitations of 'first and second digital data streams are not restricted to a set of predetermined sample rates'.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Loh into Rabenko and Oltean in order to prevent aliasing while converting from one sampling rate to another by incorporating sample rate conversion with digital mixer as taught by Loh (col.2, lines 1-14).

21. As per claim 6, Rabenko and Oltean teach all the limitations in the previous claim on which claim 6 depends but they fail to disclose sample rate converter.

Loh teaches sample rate conversion for digital system (col.2, lines 18-20 & 37-47) which reads on claim limitations 'single sample rate converter'.

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Loh into Rabenko and Oltean in order to

prevent aliasing while converting from one sampling rate to another by incorporating sample rate conversion with digital mixer as taught by Loh (col.2, lines 1-14).

22. As per claim 7, Rabenko and Oltean teach all the limitations in the previous claim on which claim 7 depends but they fail to disclose conversion of first and second digital data streams from input sample rate to predetermined sample rate in corresponding channels.

Loh teaches, 'the data processor is configured to convert the first and second digital data streams form the corresponding input sample rates to the predetermined sample rate in corresponding channels, wherein at least a portion of a plurality of processing components of the channels are common to each of the channels' (figure 7, col.5, lines 64-67, col.6, lines 1-6, 27-32, col.7, lines 19-24, col.8, lines 11-17).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Loh into Rabenko and Oltean in order to prevent aliasing while converting from one sampling rate to another by incorporating sample rate conversion with digital mixer as taught by Loh (col.2, lines 1-14).

23. Claim 19 is rejected under the same rationale as mentioned in the rejection of claim 5 above.

24. Claims 20 and 21are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) in view of Oltean (6,044,113), as applied to claims 1 & 11 above, and further in view of Midya et al. (6,665,338).

25. As per claims 20 and 21, Rabenko and Oltean teach all the limitations in the previous claims on which claims 20 and 21 depend by they fail to disclose pulse width

audio digital amplifier. Oltean teaches pulse width modulation for electronic devices (col.1, lines 21-26 & 55-57).

Midya teaches, 'pulse-width modulated digital audio amplifier' (figure 1, elements 10, 22, col.1, lines 27-29, col.2, lines 19-24).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Midya into Rabenko and Oltean in order to convert a uniformly sampled signal to naturally sampled signal which is used to produce a naturally sampled pulse width modulated signal as taught by Midya (col.1, lines 38-42).

26. Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabenko et al. (6,765,931) in views of Oltean (6,044,113) and Holland et al. (5,367,162), as applied to claims 1, 8, 9, 11, 15 & 16 above, and further in view of Loh et al. (5,621,805) (hereinafter, Loh).

27. As per claim 10, Rabenko, Oltean and Holland teach all the limitations in the previous claim on which claim 10 depends but they fail to disclose conversion of first and second digital data streams to the predetermined rate based on the estimated primary and secondary digital data rates respectively.

Loh converts input data source 1 rate (figure 7, col.6, lines 42-48) (claimed first digital data and estimated primary rate since input data source 1 has first input rate associated with) into common sampling output rate (col.6, lines 42-48) (claimed convert the first digital data stream to the predetermined rate) and data source 2 rate (figure 7) (claimed second digital data and estimated secondary rate since input data source 2

has its own input rate associated with) into common sampling output rate (col.6, lines 42-48) (figures 4, 6A & 7, col.6, lines 28-47) (claimed convert the second digital data stream and estimated secondary rate).

It would have been obvious to one of ordinary skill in the art, at the time invention was made, to implement the teachings of Loh into Rabenko, Oltean and Holland in order to prevent aliasing while converting from one sampling rate to another by incorporating sample rate conversion with digital mixer as taught by Loh (col.2, lines 1-14).

28. Claim 17 is rejected under the same rationale as mentioned in the rejection of claim 10 above.

Contact Information

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Naheed Ejaz
Examiner
Art Unit 2611

8/1/2007

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